CMOS compatible plasmonic devices for nano-integrated circuits

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Abstract

This paper presents a novel CMOS-compatible plasmonic waveguide building block , which is based on the metal-silica-silicon hybrid plasmonic waveguides. Study shows that the propagation loss of the waveguide can be as low as 0.4 dB/μm with a cross section of 100×340 nm^2. The block can be used to build various plasmonic nano-devices. As an example, a ring resonator with the ring radius of 0.91μm is demonstrated. In addition, a novel nanoparticle-based Schottky barrier Si-waveguide photodetector is presented as well. The absorption in the photodetector is dramatically enhanced due to the localized surface plasmon resonance.

1. Introduction

Integrating optical devices with electronic circuits could simultaneously achieve both ultra-compactness of electronics and the super-wide bandwidth of optics. However, the dimensions of traditional optical devices are fundamentally limited by the law of diffraction and therefore greatly limit the progress of merging photonics with electronics. Plasmonics is emerging as a promising technology platform towards enabling the deployment of small-footprint integrated circuitry, holding a great promise for chip-scale high density integration. It is also vital important to implement the plasmonic devices and circuits with existing CMOS-compatibility technology. For these purpose, we design and demonstrate novel CMOS-compatible hybrid plasmonic waveguide (HPW) and plasmonic devices to guide, manipulate and process high-bandwidth information in subwavelength scale for opto-electronic integrated circuits.

2. CMOS compatible plasmonic waveguide platform

Among different plasmonic waveguide platforms, the hybrid plasmonic waveguide has drawn substantial research interest because of the exciting potential for integrating metallic and semiconductor nanostructures to fully exploit the advantages of both metals (light concentration and high electrical conductivity) and semiconductors (light emission and photocurrent generation) [1-2]. We designed a vertical hybrid plasmonic waveguide (VHPW) as shown in Fig. 1(a) which consists of a thin layer of SiO2 film of nanometer thickness sandwiched between a subwavelength Si nanowire and a metal film with air cladding. The distribution of the power along the cross-section of structure, plotted in Fig. 1(b), demonstrates a strong confinement of the energy in the thin SiO_2 film, and therefore the VHPW exhibits better waveguiding performance than the metal-insulator-metal counterpart. Although the

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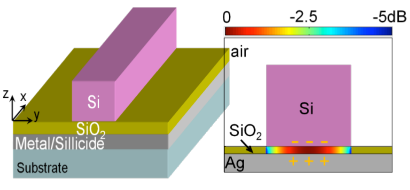
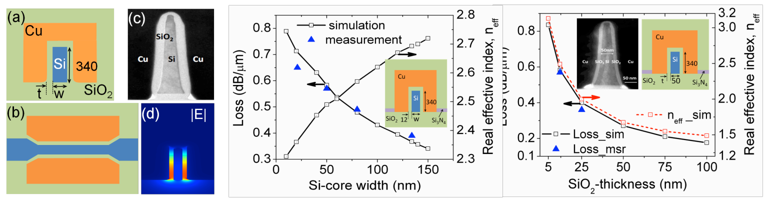
VHPW has been successful investigated with noble metals (such as Au and Ag) in literature, these metals are not compatible with the standard Si-based CMOS fabrication technology. For these purposes, the metallic materials, such as Cu, Al and sillicides have been adopted in designing various CMOS-compatible hybrid plasmonic waveguide-based devices. More specifically, we have developed a plasmonic waveguide platform based on a copper-silica-silicon (Cu-SiO_2-Si) lateral hybrid plasmonic waveguide through which a number of plasmonic devices have been designed to guide, manipulate and process high-bandwidth information in a subwavelength scale [3]. The sketch of proposed LHPW and the real TEM image of the fabricated LHPW are shown in Fig. 2(a)-(c). The distribution of the electric field intensity in the cross section of the waveguide is plotted in Fig. 2(d), which demonstrates that the LHPW can achieve high confinement in the ultrathin low-index SiO_2 layer. Several LHPWs have been numerically designed and experimentally characterized. A very good agreement between simulation and measurement of transmission loss through different dimensions of Si- and



(a) (b)

Fig 1. (a) Schematics of the proposed Si-based vertical hybrid plasmonic waveguide. (b): Power distribution (in dB) in the yz-plane of the waveguide. Light is strongly confined in the ultrasmall area with thickness of λ/1200.



(e) (f)

Fig 2.(a) Cross-section and (b) top view of the proposed Lateral hybrid plasmonic waveguide (LHPW) structures, (c)TEM image of the cross section of waveguide.(e) Propagation loss and effective index of the waveguide as a function of thickness of the Si core; a good agreement between simulation and measurement is observed. (f) Propagation loss and effective index as a function of SiO_2 thickness; the inset shows the simulated and measured waveguide.

SiO_2-layer of proposed waveguides has been observed and shown in Fig. 2(e)-(f). Our proposed LHPW provides lower loss while demonstrating similar confinement to the metal-insulator-metal waveguide.

3. Plasmonic devices for integrated circuits

Waveguide based ring resonator: Various waveguide devices including bends, power splitters and ring resonators have been designed and characterized. For example, a fully CMOS-compatible nanoscaled ring resonator (RR) has been designed and implemented experimentally based on the proposed LHPW platform. Our proposed RR is formed by a ring waveguide placed in the proximity of a straight bus waveguide (Fig. 4(a)) to allow optical coupling between them. The TEM images for the fabrication process corresponding to the mid- and final-step are shown in Fig. 4(b) and 4(c). In Fig. 4(d), we plots the transmission spectrum for a RR constructed by a LHPW platform with a Si core of width of 20 nm, a SiO_2 layer of thickness of 26 nm and covered with Cu. From the spectrum, the proposed RR demonstrate excellent performance: e.g., radii: 0.91 μm; quality factor: ~300 at $\lambda = 1.47$ um; free spectral range (FRS): ~130 nm; extinction ratio (ER) ~24 dB; insertion loss ~2.5 dB; and volume ~0.145 μm^3. In the inset of Fig. 4(d) we compare our simulated and measured transmission in the range of wavelengths from 1.52 μm to 1.62 μm. Moreover the field intensity $|E|^2$ in Fig. 4(e) demonstrates that the optical signal is efficiently guided and filtered from the input channel to the output channel at the resonant wavelength of 1.47 μm and non-resonant wavelength of 1.5 μm.

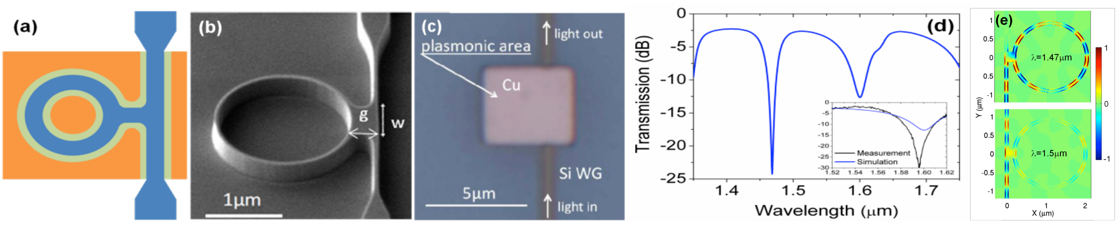


Fig 4. Ring resonators implemented with the proposed LHPW. (a) Cutting plane of the proposed structure. TEM images of the mid (b) and the final stage (c) of the ring resonator during the fabrication. (d) Simulated and measured transmission as a function of the input wavelengths. (e) Simulated electric-field at the resonant and non-resonant wavelength of 1.47 μm and 1.5 μm, respectively.

Plasmonic detectors: To realize monolithic integration of optoelectronic-circuit, an ultra-compact, high performance, and CMOS compatible detector that enables optical-to-electrical encoding is essential. The Schottky contact diode, which consists of a metallic layer on a doped Si, is considered as an alternative to Ge photodetector to detector the near-infrared signal, attributing to its large absorption coefficient and relatively low Schottky barrier Φ_B. Fig. 5(a)-(c) shows different types of NiSi Schottky Barrier Detector (SBD), amount which the structure with NiSi nanodisk array embedded in doped Si waveguide Fig 5(c) is the most promising one, because of the strong field enhancement around metallic nanodisks and therefore improved photo absorption efficiency [4].

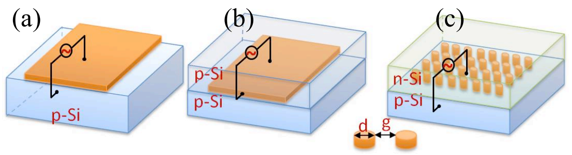


Fig 5 Schematics of 3 types of Si-Wg integrated SBD (a) metallic thin film on top (b) metallic thin film in the middle, and (c) nanodisk arrays embed in the middle

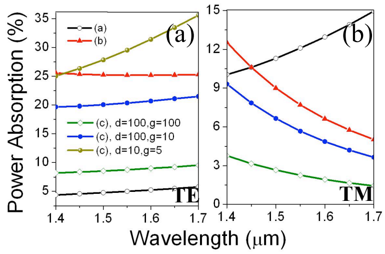


Fig 6 Power absorption for both (a)TE and (b)TM modes

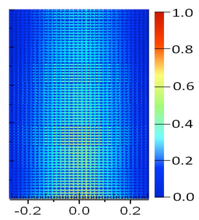


Fig 7 $|E|^2$ across the center of nanodisk

Fig. 6 shows the calculated total power absorption in near-infrared region (1.4μm to 1.7μm) for both TE and TM modes. The absorption efficiency for TE mode is in general higher than that for TM mode, except for the structure in Fig. 6(a). The total power absorption can be improved by more than 5 times by shifting the NiSi layer from top to the center of the Si waveguide. Fig. 7 plots the electric field intensity distribution along the center of the NiSi, the fields are strongly enhanced at the vicinity of the NiSi nanodisk. Hot carriers are then generated surrounding the nanodisk and then quickly sweep to the n-Si and p-Si region to the external circuit to form photocurrent. Our study also shows that by replacing NiSi nanodisk by Al nanodisk, we can further improve the total absorption up to 96%. In short, we propose a novel surface plasmon enhanced Schottky Barrier Detector structure that enables a fully CMOS compatible photonic-electronic integrated circuit.

4. Conclusion

We have demonstrated various CMOS compatible plasmonic devices for optical-electronic integrated circuits. The devices include the Cu/SiO2/Si/SiO2/Cu waveguide platform, waveguide ring resonators, and nanoparticle-based Schottky barrier Si-waveguide photodetectors. These devices have nanoscale footprint and show excellent performance. We believe this work will be useful for the integration of nanoscale electronic-photonic integrated circuits.

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